AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes a change to Fig. 1(b) to replace reference number "100" with "100b".

Attachment: Replacement sheet

REMARKS

Claims 1-24 have been examined, with claims 1-8, 10-14, 19, and 20 rejected, and claims 9, 15-18, and 21-24 objected to.

Applicant thanks the Examiner for the indication of allowable subject matter in claims 9, 15-18, and 21-24.

The specification and claim 1 have been amended to correct minor informalities.

Claims 1-8, 10-14, 19, and 20[1] have been rejected under 25 YSC 102(b) as being anticipated by Williams et al. (U.S. Patent No. 5,530,837; hereinafter, "Williams"). Applicant respectfully traverses this rejection for the reasons set forth below.

Independent claim 1 is directed to a cache unit having a first memory tower (320_T0), which has a first way sub-tower and a second way sub-tower, and a second memory tower (320_T1), which has a first way sub-tower and a second way sub-tower. A first cache line (0) of the cache unit includes a first plurality of data segments (HW_0_0, HW_0_2, HW_0_4, and HW_0_6) in the first way sub-tower of the first memory tower and a second plurality of data segments (HW_0_1, HW_0_3, HW_0_5, and HW_0_7) in the first way sub-tower of the second memory tower.

Williams is directed to a system for interleaving memory transactions into a plurality of banks. For example, Fig. 1C illustrates a two-way interleaved memory system having two equal size banks 31 and 32.

Williams does not teach a memory tower, which has a first way sub-tower and a second way sub-tower, as required by the claimed invention. Rather, Williams teaches

[1] The statement of the rejection includes claim 21, but it is clear from reading the Office Action as a whole that the Examiner did not intend to include this claim.

simple memory banks 31, 32. Since Williams does not teach the claimed memory tower, it necessarily follows that Williams can not teach a first cache line with a first plurality of data segments in a first way sub-tower of a first memory tower and a second plurality of data segments in a first way sub-tower of a second memory tower, as required by the claimed invention. Thus the claims are patentable over Williams for at least this reason.

Independent claim 13 also recites storing a first plurality of data segments of a first cache line in a first way sub-tower of a first memory tower, and storing a second plurality of data segments of the first cache line in a first way sub-tower of a second memory tower, and is therefore not anticipated by Williams for the same reasons as discussed above with respect to independent claim 1.

Further, independent claim 13 recites storing a first plurality of data segments of a second cache line in a second way sub-tower of the first memory tower, and storing a second plurality of data segments of the second cache line in a second way sub-tower of the second memory tower. Again, since Williams does not teach the claimed memory tower, it necessarily follows that Williams also can not teach this claimed feature. Thus the claims are patentable over Williams for this additional reason.

Similar to independent claim 13, independent claim 19 recites means for storing a first plurality of data segments of a first cache line in a first way sub-tower of a first memory tower, and means for storing a second plurality of data segments of the first cache line in a first way sub-tower of a second memory tower. Independent claim 19 also recites means for storing a first plurality of data segments of a second cache line in a second way sub-tower of the first memory tower, and means for storing a second plurality of data segments of the second cache line in a second way sub-tower of the second

memory tower. Claim 19 is therefore not anticipated by Williams for the same reasons as discussed above with respect to independent claim 13.

Claims 2-8 and 10-12 depend from claim 1, claim 14 depends from claim 13, and claim 20 depends from claim 19. Applicant submits that claims 2-8, 10-12, 14, and 20 are patentable for at least the same reasons as discussed above with respect to their respective base claims. Applicant therefore respectfully requests reconsideration and withdrawal of the prior art rejection.

In view of the above, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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